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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/512,149	02/23/2000	Vishnu K Agarwal	MI22-1322	3457

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EXAMINER
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ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 05/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/512,149	AGARWAL, VISHNU K	
	Examin r	Art Unit	
	Marcos D. Pizarro-Crespo	2814	

-- The MAILING DATE of this communication appears on the cover sh et with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4-14 and 56-103* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *63-70,72-77,79,82 and 94-98* is/are allowed.

6)☒ Claim(s) *1,4-14,56-62,71,78,80,81,83-93 and 99-103* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Attorney's Docket Number: MI22-1322
Filing Date: 2/23/2000
Claimed Foreign Priority Date: none
Applicant(s): Agarwal
Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the amendment in paper no. 37 filed on 4/1/2004.

Acknowledgment

1. The amendment in paper no. 37, filed on 4/1/2004, responding to the Office action in paper no. 35, mailed on 10/1/2003, has been entered. The present Office action is made with all the suggested amendments being fully considered. Accordingly, pending in this office action are claims 1, 4-14, and 56-103.

Specification

2. The amendment in paper no. 37, filed on 4/1/2004, is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: the paragraph beginning at line 20 on page 12 now describing the openings in figure 9 as comprising trenches.

3. Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 71 and 78 are rejected under 35 U.S.C 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

6. Claim 71 describes a trench within which a first electrode layer of a capacitor is formed. The description in the original disclosure fails to support this limitation in the claim. Although the specification (see, *e.g.*, pp.12/ll.24-pp.13/ll.3) describes an opening within which a first capacitor electrode is formed, it fails to describe said opening as a trench.

7. Claim 78 describes a first electrode layer comprising a monolithic unitary material. The description in the original disclosure fails to support this limitation in the claim. The specification (see, e.g., pp.7/ll.4-7) listed several materials from which to make the first electrode layer. A *monolithic unitary material*, however, is not one of them.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 4-11, 13, 14, 56, 80, and 90 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ramakrishnan (US 5192871) in view of Motorola (US 5943580).

10. Regarding claim 1, Ramakrishnan shows (see, *e.g.*, fig. 2) most aspects of the instant invention including an integrated circuitry comprising a capacitor comprising:

- a first capacitor electrode **14**
- a second capacitor electrode **20**
- a high-K capacitor-dielectric region between the capacitor electrodes comprising:
  - a high-K substantially-amorphous-material layer **18**
  - a high-K substantially-crystalline-material layer **16** over the amorphous-material layer **18**

wherein the crystalline and the amorphous layers may be made out of different chemical compositions (see, *e.g.*, col.2/ll.46-50).

Ramakrishnan, however, fails to disclose that the crystalline-material layer is 70-90% crystalline. Nonetheless, the degree of crystallinity (or amorphicity) of a dielectric layer is considered a parameter subject to optimization and it is not patentable unless unobvious or unexpected results are obtained from it.

Motorola (see, *e.g.*, col.3/ll.5-15), for example, teaches that by selecting the crystallinity percentage of dielectric layers one is able to create capacitors with a wide range of dielectric constants on a single substrate. In other words, controlling the degree of crystallinity of Ramakrishnan's dielectric layer gives the skilled artisan control over the dielectric constant of the capacitor dielectric.

Consequently, it would be an obvious matter of design choice for one of ordinary skill in the art at the time the invention was made to select the degree of crystallinity of Ramakrishnan's dielectric layer since this is a variable of importance subject to routine experimentation and optimization that, as taught by Motorola, will give control over the dielectric constant of the capacitor dielectric, and it is not inventive to discover the optimum or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235.

In addition since the applicant has not established the criticality (see next paragraph) of the degree of crystallinity stated, it would have been obvious to one of ordinary skill in the art to use these values in the capacitor of Ramakrishnan/Motorola.

CRITICALITY

11. The specification contains no disclosure of either the critical nature of the claimed arrangement or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical. *In re Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

12. Regarding claim 4, Ramakrishnan shows at least one of the first and second electrodes comprising a metal (see, *e.g.*, col.1/ll.60).

13. Regarding claims 5-9, 11, 13, and 14, Ramakrishnan's shows (see, *e.g.*, fig. 2):

- the capacitor over a semiconductor substrate **12**
- the dielectric layer received between the first and second capacitor plates **14 20**
- the amorphous layer **18** contacting the first capacitor electrode **14**
- the crystalline layer **16** contacting the second capacitor electrode **20**
- the dielectric layer as the only capacitor dielectric region between the capacitor electrodes **14 20**

- the amorphous material layer **18** received between the semiconductor substrate **12** and the crystalline dielectric layer **16**

14. Regarding claims 10, 56, and 80, see the comments stated above in paragraph 10 regarding claim 1, which are considered repeated here.

15. Regarding claim 90, Ramakrishnan (see, *e.g.*, col.2/ll.68-col.3/ll.3) teaches that the amorphous material is provided in an amount effective to reduce leakage current through the crystalline material.

16. Claims 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ramakrishnan and Motorola, as applied to claims 1 and 11 above, and further in view of Graettinger (US 5844771).

17. Ramakrishnan/Motorola shows most aspects of the instant invention (see, *e.g.*, paragraphs 10-15 above), except for a capacitor wherein the semiconductor substrate comprises bulk monocrystalline silicon. Graettinger (see, *e.g.*, col.1/ll.20-24), on the other hand, teaches that in the processing of integrated circuits the substrate typically comprises monocrystalline silicon.

It would have been obvious at the time of the invention to one of ordinary skill in the art to have the substrate of Ramakrishnan/Motorola comprising monocrystalline silicon, as suggested by Graettinger, because in the processing of integrated circuits the substrate is typically monocrystalline silicon.

18. Claims 57-59 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ramakrishnan/Motorola in view of Narui (US 6201728) and Merchant (US 6235594).

19. Ramakrishnan/Motorola shows most aspects of the instant invention (see, *e.g.*, paragraphs 10-15 above), except for an insulative layer between the substrate and the capacitor electrodes. Narui (see, *e.g.*, col.7/ll.47-55), on the other hand, teaches that an insulating layer formed between the substrate and the capacitor insulates the electrodes thereof and hence the leakage current is minimized. Merchant further teaches that this insulation layer is typically silicon dioxide (see, *e.g.*, col.2/ll.15-20, col.3/ll.61-col.4/ll.11).

Accordingly, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time of the instant invention to include a silicon-dioxide insulative film between Ramakrishnan/Motorola's substrate and his capacitor, as suggested by Narui and Merchant, to minimize the leakage current.

20. Claims 60-62 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ramakrishnan/Motorola in view of Eguchi (US 5442585) and Shrivastava (US 5557122).

21. Ramakrishnan/Motorola shows most aspects of the instant invention (see, *e.g.*, paragraphs 10-15 above), except for the specific capacitor-dielectric thickness claimed by the applicants *i.e.*, an amorphous dielectric thickness of 20-250Å, a crystalline dielectric thickness of 20-90Å, and a capacitor-dielectric region of 40-500Å.

Ramakrishnan, however, shows that the crystalline-dielectric layer may have a thickness of 100Å (see, *e.g.*, col.3/ll.44) and that the amorphous-dielectric layer should be as thin as possible in order to prevent degradation of the capacitor performance (see, *e.g.*, col.4/ll.20-26). Although Ramakrishnan/Motorola does not specify the same thicknesses as those claimed by the applicants, thickness differences are considered

obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes.

Shrivastava, for example, teaches that the capacitor-dielectric thickness is a design variable that if reduced will increase the capacitance of the capacitor (see, *e.g.*, col.2/ll.59-63). Likewise, Eguchi teaches that in order to increase the capacitance of a capacitor, the thickness of the capacitor dielectric should be reduced; however, if the film is made too thin, the performance of the capacitor deteriorates (col.1/ll.44-48).

Accordingly, it would be an obvious matter of design choice to select a suitable thickness for the capacitor-dielectric layers of Ramakrishnan, as taught by Shrivastava and Eguchi, since the capacitor-dielectric thickness is a variable of importance subject to routine experimentation and optimization and it is not inventive to discover the optimum or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235. Furthermore, it appears that the thickness differences between Ramakrishnan/Motorola's dielectric layer and the one claimed produce no functional differences and therefore would have been obvious. Note *In re Leshin*, 125 USPQ 416.

In addition, since the applicant has not established the criticality (see paragraph 11 above) of the thickness stated, it would have been obvious to one of ordinary skill in the art to use these values in the capacitor of Ramakrishnan/Motorola.

22. Claim 81 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ramakrishnan/Motorola in view of Yanagita (US 6376332).

23. Ramakrishnan/Motorola shows most aspects of the instant invention (see paragraphs 10-15 above), except for the integrated circuitry formed over a

semiconductor-on-insulative substrate. Yanagita (see, *e.g.*, col.1/ll.25), on the other hand, teaches that doing so will increase the operating speed of the circuitry.

Consequently, it would have been obvious at the time of the invention to one of ordinary skill in the art to form the integrated circuitry of Ramakrishnan/Motorola over a semiconductor-on-insulative substrate, as suggested by Yanagita, to increase the operating speed of the circuitry.

24. Claim 91 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ramakrishnan/Motorola in view of Mundy (US 3755692).

25. Regarding claim 91, Ramakrishnan/Motorola shows most aspects of the instant invention (see, *e.g.*, paragraphs 10-15 above), except for the capacitor comprising a portion of a logic circuitry. Mundy (see, *e.g.*, col.4/ll.6-8), on other hand, teaches that adding the capacitor of Ramakrishnan/Motorola to a logic circuit enhances the voltages therein and reduces the operating time.

It would have been obvious to one of ordinary skill in the art to add the capacitor of Ramakrishnan/Motorola to a logic circuit, as suggested by Mundy, to enhance the voltages in the circuit and to reduce the operating time.

26. Claims 92 and 93 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ramakrishnan/Motorola in view of Burgess (US 3691537).

27. Regarding claims 92 and 93, Ramakrishnan/Motorola shows most aspects of the instant invention (see, *e.g.*, paragraphs 10-15 above), except for the capacitor comprising a portion of a DRAM circuitry. Burgess (see, *e.g.*, abstract), on the other

hand, teaches that, in a DRAM, connecting the capacitor of Ramakrishnan/Motorola to the storage node will increase the transconductance of the read transistor.

It would have been obvious at the time of the invention to one of ordinary skill in the art to add the capacitor of Ramakrishnan/Motorola to a DRAM circuitry, as suggested by Burgess, to increase the transconductance of the read transistor.

Claim Rejections - 35 USC § 102

28. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

29. Claim 83 is rejected under 35 U.S.C. 102(b) as being anticipated by Mihara.

30. Regarding claim 83, Mihara shows (see, *e.g.*, fig. 16) all aspects of the instant invention including an integrated circuitry comprising:

- a substrate **62** having insulative material **66** formed over the substrate **62**
- an opening formed in the insulative material **66**
- a capacitor comprising:
  - a first electrode layer **91** formed within the opening
  - a high-K dielectric layer **96** formed over the first electrode layer **91** and within the opening
  - a second electrode layer **97** formed over the high-K dielectric layer **96**

wherein the high-K dielectric layer **96** may comprise a portion of amorphous material and a portion of crystalline material (see, *e.g.*, col.11/ll.8-18).

31. Claims 84-86 and 88 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mihara in view of Motorola.

32. Regarding claims 84-86 and 88, Mihara shows most aspects of the instant invention (see paragraph 30 above). He, however, fails to disclose a specific degree of crystallinity (or amorphicity) for the crystalline portion and/or the amorphous portion of the dielectric layer. Nonetheless, the specific degrees of crystallinity (or amorphicity) of the dielectric layer claimed by the applicant are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from them.

Motorola (see, *e.g.*, col.3/ll.5-15), for example, teaches that by selecting the crystallinity percentage of dielectric layers one is able to create capacitors with a wide range of dielectric constants on a single substrate. In other words, controlling the degree of crystallinity of Mihara's dielectric layer gives the skilled artisan control over the dielectric constant of the capacitor dielectric.

Consequently, it would be an obvious matter of design choice for one of ordinary skill in the art at the time the invention was made to select the degree of crystallinity (or amorphicity) of Mihara's dielectric layer since this is a variable of importance subject to routine experimentation and optimization that, as taught by Motorola, will give control over the dielectric constant of the capacitor dielectric, and it is not inventive to discover the optimum or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235.

33. Claim 103 is rejected under 35 U.S.C. 103(a) as being unpatentable over Mihara in view of Venkatraman (US 6093966).

34. Mihara shows most aspects of the instant invention (see, *e.g.*, paragraph 30 above), except for the outermost portion of the insulating material comprising an antireflective coating layer. Venkatraman (see, *e.g.*, col.4/ll.54-59), on the other hand, teaches that providing Mihara's outermost portion of the insulating material with an antireflective layer will minimize the reflections from underlying features during the subsequent photolithographic definition of openings and via holes, so that a uniform distribution of the critical dimensions of these features is obtained.

It would have been obvious at the time of the invention to one of ordinary skill in the art to provide Mihara's outermost portion of the insulating material with an antireflective layer, as suggested by Venkatraman, so that a uniform distribution of the critical dimensions of the opening is obtained.

35. Claims 83, 87, 89, 99, 101, and 102 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schuele in view of Ramakrishnan.

36. Regarding claim 83, Schuele shows (see, *e.g.*, fig. 6) most aspects of the instant invention including an integrated circuitry comprising:

- a substrate **30** having insulative material **37** formed over the substrate **30**
- an opening formed in the insulative material **37**
- a capacitor **75** comprising:
  - a first electrode layer **50** formed within the opening
  - an insulating layer **60** formed over the first electrode layer **50** and within the opening
  - a second electrode layer **70** formed over the insulating layer **60**

Schuele, however, fails to show that the insulating layer **60** is formed of a high-K material comprising a crystalline portion and an amorphous portion. Ramakrishnan, on the other hand, teaches it would be highly advantageous to Schuele's capacitor insulating layer to have a high-K dielectric material having a crystalline portion and an amorphous portion. This structure will provide the sought-after high-dielectric constant that characterizes crystalline capacitor dielectrics, while at the same time preventing the migration of foreign materials that may adversely affect the dielectric constant of the capacitor-insulating layer. See, *e.g.*, Ramakrishnan, col.1/ll.45-50,col.2/ll.35-57, and col.3/ll.23-30.

Consequently, it would have been obvious at the time of the invention to one of ordinary skill in the art to have a high-K dielectric material having a crystalline portion and an amorphous portion for the capacitor insulating layer of Schuele, as suggested by Ramakrishnan, to protect the dielectric properties of the layer.

37. Regarding claim 87, Ramakrishnan shows that the high-K dielectric layer may comprise Ta_2O_5 (see, *e.g.*, col.3/ll.53).

38. Regarding claim 89, Ramakrishnan shows (see, *e.g.*, col.2/ll.48) that the portion of amorphous material and may comprise a different material than that of the portion of crystalline material.

39. Regarding claim 99, Ramakrishnan (see, *e.g.*, col.2/ll.68-col.3/ll.3) teaches that the amorphous material is provided in an amount effective to reduce leakage current through the crystalline material.

40. Regarding claims 101 and 102, Schuele shows that the capacitor comprises a portion of a DRAM circuitry.

41. Claim 100 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schuele/Ramakrishnan in view of Wu (US 5998247).

42. Schuele/Ramakrishnan shows that a DRAM device includes a capacitor **75** (see, *e.g.*, fig. 6). However, they fail to the capacitor comprising a portion of a logic circuitry. Wu (see, *e.g.*, col.1/ll.12-15), on the other hand, teaches that logic circuits with DRAM devices are demanded as high performance devices that reduce power consumption and increase packing density.

It would have been obvious at the time of the invention to one of ordinary skill in the art to include the capacitor of Schuele/Ramakrishnan into a logic circuit, as suggested by Wu, to reduce power consumption.

Allowable Subject Matter

43. Claims 63-70, 72-77, 79, 82, and 94-98 are allowed.

Response to Arguments

44. The applicants argue:

Regarding the 112, first paragraph, rejection against claim 71, such claim recites an opening comprising a trench. Wolf, vol.2, pp.600-609, illustrates exemplary openings referred to as trenches. The openings of Wolf are similarly configured as shown in figure 9 of Applicant's originally filed application, and therefore, at least this figure 9 provides support for a trench.

The examiner responds:

The applicant may have intended the openings 130 and 131 in figure 9 to be trenches but never said so in the original specification. The pictures in Wolf are showing trench capacitors and, as acknowledge by the applicant, Wolf specifically

describe the openings as trenches, something the applicant did not do in the original disclosure. The applicants only disclosure in the specification is that the capacitor is formed within container openings 130 131 (see, *e.g.*, pp.12/ll.24-pp.13/ll.6).

The fact that the cross sectional views across the openings look alike in the drawings does not mean that they are the same. A cross sectional view of a square pyramid may look like that of a cone although they have totally different shapes.

45. The applicant argues:

> The subject matter of the claim need not be described literally in order to satisfy the description requirement as long as the skilled artisan may reasonably convey that the inventor had possession at that time of the later claimed subject matter. The originally filed application (see, *e.g.*, pp.1) discusses two exemplary types of capacitors, "cylindrically stacked or trench structures". Therefore, Applicant submits that such a disclosure would reasonably convey to the artisan skilled in the semiconductor art that Applicant had possession of the subject matter to an opening that comprises a trench. Figure 9 provides the required support for claim 71, and therefore, no new matter is added for amending the specification.

The examiner responds:

On page 1, the applicant describes that there are two types of prior-art three-dimensional capacitor structures, trenched and stacked capacitors. However, that does not mean that the openings in figure 9 are trenches or that the skilled artisan will so understand. The skilled artisan would have readily understood that page 1 of the original specification was describing that there are two different types of 3-dimensional capacitors. See, *e.g.*, par[008] of US2002/0176314, par[008] of US2002/0140020, par[007] of US 2002/0081841, and col.1/ll.50-59 of US6274423, all of which are currently assigned to Micron, and establishing that stacked capacitors and trench capacitors are two different types of capacitor structures. In fact, in figure 11 of US6274423, Micron is showing a *stacked* capacitor sharing similar cross sectional features to those in figure 9 of the instant application. Note, for example, that both

capacitors are formed on top of the transistors. A trench capacitor, on the other hand, is formed in a trench formed *in* the substrate, as *all* the drawings in Wolf show. Now, a stacked capacitor could have been formed in a *trench* opening in an insulating layer on top of the transistor and still be a stacked capacitor. However, such a *trench* opening was not described in the original disclosure of the instant application. As described on page 12/ll.24-pp.13/ll.1, Figure 9 shows a stacked capacitor formed in container openings 130 131. The original specification, however, fails to describe the openings 130 131 as a trench openings.

46. The applicant argues:

Motorola fails to provide any teachings about specific crystallinity ranges. No design choice or routine experimentation can be performed without some basic teachings about specific ranges on which to base the design choice and routine experimentation.

The examiner responds:

The prior art clearly teaches that the degree of crystallinity (or amorphicity) of a dielectric layer is a parameter subject to optimization and; therefore, it is not patentable unless unobvious or unexpected results are obtained from it. *In re Aller* 220 F.2d 454, 456, 105 USPQ 233, 235 CCPA 1955.

Motorola (see, *e.g.*, col.3/ll.5-15), for example, teaches that by selecting the crystallinity percentage of dielectric layers one is able to create capacitors with a wide range of dielectric constants on a single substrate. In other words, controlling the degree of crystallinity of Ramakrishnan's dielectric layer provides the skilled artisan with the ability to control the dielectric constant of the capacitor dielectric.

Consequently, it would be an obvious matter of design choice for one of ordinary skill in the art at the time the invention was made to select the degree of crystallinity for

a dielectric layer since this is a variable of importance subject to routine experimentation and optimization that, as taught by Motorola, will provide control over the dielectric constant of the capacitor dielectric, and it is not inventive to discover the optimum or workable ranges by routine experimentation. *In re Aller*, 220 F.2d 454, 105 USPQ 233, 235.

47. The applicant argues:

> The skilled artisan would not modify the crystalline percentage of Ramakrishnan's crystalline dielectric layer since he teaches away from forming a partially crystalline layer. He clearly discloses that the dielectric layer 16 should have the highest possible dielectric constant because crystalline films have higher dielectric constants than their amorphous or partially crystalline films counterparts (see, *e.g.*, col.2/ll.35-40).

The examiner responds:

"A known or obvious composition does not become patentable simply because it has been described as somewhat inferior to some other product for the same use." *In re Gurley*, 27 F.3d 551, 554, 31 USPQ2d 1130, 1132 (Fed. Cir. 1994). In the instant case, Ramakrishnan (see, *e.g.*, col.2/ll.34-40) teaches that, to obtain the highest dielectric constant, the capacitor dielectric film should have the highest possible crystallinity. That is not to say that amorphous or partially crystalline dielectrics are not useful, as crystalline dielectric layers also have their flaws (see, *e.g.*, Ramakrishnan/col.2/ll.40-46). On the other hand, Ramakrishnan (see, *e.g.*, Ramakrishnan/col.2/ll.52--57) also teaches that amorphous dielectric layers have a more uniform, defect-free structure that prevents penetration of conductive foreign materials into the film. That is not to say that crystalline dielectrics are not useful anymore since as noted above they are.

Besides, the teachings of Ramakrishnan are those of the applicant himself. The applicant teaches that the crystalline layer should have the highest possible crystallinity, most preferably above 98% (see, *e.g.*, pp.7/ll.21). However, the claimed crystallinity is not the highest possible but somewhat lower, *i.e.*, 70-90%, which according to the specification is acceptable but nonetheless lower. The applicant must have a motivation to do so, otherwise it wouldn't be claimed. Motorola also provides a motivation to do so to Ramakrishnan's crystalline dielectric layer (see, *e.g.*, paragraph 11 above).

Conclusion

48. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

49. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

50. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(703) 872-9306**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

51. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(571) 272-1716** and between the hours of 9:30 AM to 8:30 PM (Eastern Standard Time) Monday through Thursday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy, can be reached on (571) 272-1705.

52. Any inquiry of a general nature or relating to the status of this application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

53. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/310, 438/240, 361/313	5/8/2004
Other Documentation:	
Electronic Database(s): EAST (USPAT, EPO, JPO)	5/8/2004

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3/4/2003